PCI to PMC (PCI Mezzanine Card) Adapter

Hardware Manual

July 23, 2008

Revision 1.2

Amfeltec Corp.
35 Fifefield dr.
Maple, ON L6A 1J2

www.amfeltec.com

Contents

Figures

Tables

1 About this Document

1.1 Purpose

This document describes Hardware installation, features, specification and operation for AMFELTEC PCI to PMC (PCI Mezzanine Card) Adapter.

1.2 Feedback

AMFELTEC makes every effort to ensure that the information contained in this document is accurate and complete at time of release. Please contact AMFELTEC if you find any errors, inconsistence or have trouble understanding any part of this document.

To provide your feedback, please send an email to support@amfeltec.com

Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	January 05, 2008
1.1	Minor updates	January 29, 2008
1.2	Software description is moved into separate document.	July 23, 2008

2 General Description

2.1 Introduction

The PMC bus adapter is a Universal high-speed 32 bit PCI bus adapter with integrated logic to support debugging and verification of PMC (PCI Mezzanine Card) cards (referred as UUT, Units-Under-Test). The UUT is plugged-in to the motherboard slot through the adapter.

The adapter uses bus switches to support two types of signal environments: 5V and 3.3V. The bus switches also allow you to disconnect the UUT PCI card from the motherboard without shutting down the system (Hot swapping mode). This flexibility minimizes the testing time and protects the motherboard from unexpected damages.

The adapter supports two ways of feeding the secondary PCI bus with power: internally, through the motherboard PCI slot, and from an external power supply. The external power supply has to provide 5V and +12V voltages to satisfy all PCI needs:

5V, +12V, -12V, 3.3V and VIO (configurable as 5V or 3.3V).

The adapter fully protects your UUT and host system from unnecessary damage by providing both monitoring and limiting of currents and voltages.

The adapter includes logic (based on the Xilinx CPLD XC9536XL-10) for debugging and verification purposes:

- FPGA Byte blaster functionality supporting different types of the FPGAs (like Xilinx, Altera, Atmel, Lattice) through the external cable
- Master I2C and SPI interfaces

The CPLD logic can be customized for the client's needs. The standard package of the adapter includes full schematics and logic for CPLD.

All these functions communicate with the computer through a standard parallel bus interface. The same interface can be used to update or to load customer’s specific functions into the on- board CPLD.

The adapter has two test-point headers of all PCI bus signals for logic analyzer hookup. It has an option of supporting plug-in high density logic analyzer adapters (like Agilent E5339A, E5346A, and E5351A). The high-density adapter is specially designed to connect a Logic Analyzer to the adapter in systems where space between PCI cards is limited (required minimal space is 20.32 mm).

The adapter supports two types of the computer boxes: the 2U and the standard profiles. The uniqueness of this mechanical design is that in the both profiles it gives you improved access to the bracket-based connectors of your UUT card.

The adapter was designed based on the many years of development experience and has many features that are very useful for development and production support of different types of FPGA-based PCI cards.

Figure 1: PCI to PMC Adapter

3 Specifications/Features

3.1 Power

- Visualization of UUT powers - 5 Volt, 3.3V, +12V and – 12V (Green LEDs)
- Over loading Protection (OLP) on the UUT 5V, 3.3V, +12V and -12V supplies
- Under-voltage protection (UVP) on the UUT 5V, 3.3V, +12V
- UUT power failure protection (in case OLP or UVP red LED indicates failure)
- UUT Power selection via jumper 5V or 3.3V
- 32 Bit Universal Primary PCI Slot and universal UUT PMC connector (based on the IEEE Std. 1386.1-2001)
- eX10_PMC can be powered from primary PCI or from external power supply (define by Jumpers block, can be used in any computer power supply with standard IDE interface power connector)
- eX10_PMC implements PCI signal level conversion for connection support of 3.3 V UUT to 5V primary PCI bus
- UUT hot swapping capability

3.2 Logic

- Supports Byte Blaster functionality for different FPGAs: Xilinx, Altera, Lattice and Atmel
- Converts parallel interface signals to/from I2C or SPI bus signals
- Supports operation with voltages from 1.2V – 5.5 V

3.3 Debugging Support

- The Extender has 2 brackets to support normal and 2U computer boxes
- All primary PCI signals are connected to 2x2.5 mm header to simplify connection with Logic Analyzer or Oscilloscope
- An additional adapter supports connection between 2x2.5 mm header and high density HP Logic Analyzer probe
- Makes it possible to access the PCI based JTAG interface of the UUT

3.4 Power Limits

Power	Threshold for under voltage monitoring	Maximum current for Over voltage protection	Comments
+3.3V	+2.74V min.	4.8 A	
+5V	+4.42V min.	4.5 A	
+12V	+10.5V min.	0.8 A	
-12V	Not available	0.2 A	In case that adapter taking power from PCI connector and PCI connector doesn't provide -12Volt power, jumper JP6 has to be short.

Table 1: Power Limits

4 Installation

4.1 Hardware

- To install the PCI adapter power off the host computer. The shipped package includes two types of brackets: low and high profile. If you like to change the brackets, you need to unscrew the installed bracket from the connector J4 and replace by another bracket.
- The eX10_PMC PCI adapter is a universal solution for debugging different types of PMC devices. In order to properly configure the adapter, please refer to Table 4 (jumpers JP5, JP11, JP12).
- The adapter has integrated Universal Byte Blaster. If you are going to use Byte Blaster, please refer to Table 3 or Appendix B (switch SW2) to set the correct mode of operation.
- Select power source for UUT. The adapter provides two options for selecting proper power source: internal power from the primary PCI bus and external power supply. In order to select the power source, refer to Table 4 (JP1, JP2, JP3, JP8 and JP9).
- Install the adapter into a PCI slot. Important Note: **Secure the adapter using a screw in the metal bracket!**
- Install UUT board into adapter.
- In case you are using external power supply you have to turn it on **first** (before powering up the computer). Then, set switch SW1 to position ON (enable power) for secondary PCI bus and UUT.

Now, you can power-up the host computer.

BE SURE THAT FOUR GREEN LEDS (D1, D3, D4 and D5) ARE ON!

4.2 Software

- Hot swapping software for saving and restoring PCI configuration for UUT for hot-swap operation (refer to *eX10 Software Manual for more details*)
- I2C master write/read software
- Supported operating systems: Windows, Linux, FreeBSD

5 Operation

In case you see the red led is ON please turn off your computer and check the adapter configuration jumpers or UUT device for power shortage.

5.1 Hot-Swap Support

Perform hot swapping with a certain degree of carefulness. Remember that PCI configuration won't be loaded or automatically updated on insertion of a new UUT device unless you use the supplied HOT SWAP software to reload the UUT's PCI configuration.

IMPROPER USE OF HOT-SWAP FEATURE CAN CAUSE THE SYSTEM TO CRASH OR THE SYSTEM CAN BECOME UNSTABLE!

5.1.1 Remove UUT Device

The following steps describe detail sequence for removing UUT device:

1. On fully operated systems save UUT PCI configuration into a file (refer to Software Manual for *more details*)
2. Unload all device drivers from the system that are using your UUT device
3. Set the switch SW1 to "OFF" (disable power)
4. Now, you can remove UUT device from the secondary PCI connector

5.1.2 Install UUT Device

The following steps describe detail sequence for installing UUT device back to the system:

1. Verify that SW1 is in position "OFF"
2. Plug in UUT device into the secondary PCI connector
3. Set the switch SW1 to "ON" (enable power)
4. Restore PCI configuration for the UUT device

Now, the UUT device is ready for use!

6 Hardware Description

6.1 Board Layout

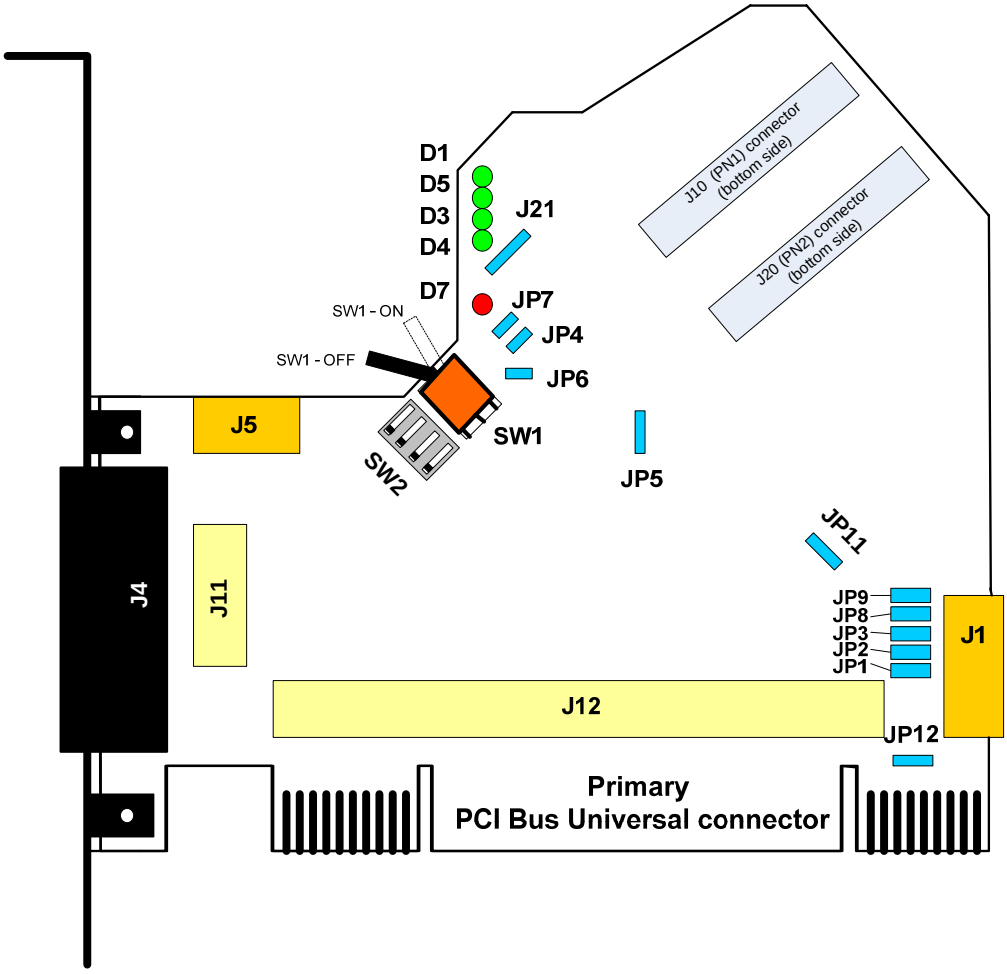


Figure 2: Board Layout

6.2 LEDs

Name	RefDes	Color	Usage
+3.3 Volt	D1	Green	3.3Volt power on the UUT

-12 Volt	D5	Green	-12Volt power on the UUT
+ 5 Volt	D3	Green	+5Volt power on the UUT
+ 12 Volt	D4	Green	+12Volt power on the UUT
+ 5 Volt	D13	Green	+5Volt power for the UUT from Primary PCI or from external connector
Power Fail	D7	Red	UUT power Fail (In case overload or under voltage)

Table 2: LEDs

In case that “Power Fail” LED is ON (overload or under voltage condition happens) it is necessarily to toggle on UUT power switch SW1 to reset the fail condition.

6.3 Switches

Name	RefDes	Type	Usage
UUT Power ON/OFF	SW1	Toggle x 1	Power switch for the UUT. In case Power OFF – all PCI signals from the Primary PCI bus are disconnected from the UUT (Hot swapping)
MODE	SW2	Toggle x 4	Four toggle switches define adapter logic between Parallel interface and UUT download interface

Table 3: Switch

Following table shows setting for the different SW2 switch settings.

1	2	3	4	Usage
ON	ON	ON	ON	Test mode for update CPLD logic itself (XC9536XL-10VQ44)
ON	ON	ON	OFF	JTAG / Parallel download interface for Xilinx
OFF	ON	ON	OFF	JTAG / Parallel download interface for Altera
ON	OFF	ON	OFF	JTAG / Parallel download interface for Lattice
OFF	OFF	ON	OFF	Download interface for ATMEL
ON	ON	OFF	OFF	Master SPI interface
OFF	ON	OFF	OFF	Master I2C interface
ON	OFF	OFF	OFF	SPARE mode
OFF	OFF	OFF	OFF	SPARE mode

Table 4: Switch SW2

6.4 Jumpers

RefDes	Type	Usage
J21	4 pins jumper	Ground pins for the Test Equipment connection
JP7	2 pins jumper	Has to be closed to provide -12 Volt power to UUT
JP4	2 pins jumper	Has to be closed to provide +12 Volt power to UUT
JP6	2 pins jumper	Has to be closed if UUT power source (Primary PCI or External power supply) doesn't have -12 Volts
JP5	3 pins jumper	1-2 pins have to be connected in case UUT power source (Primary PCI or External power supply) doesn't have +12 Volts
JP12	3 pins jumper	If 2-3 pins are closed then all 5 volt signals from Primary PCI will be converted to 3.3 volt signals. (To support 3.3 volts UUT). If pins 1-2 are closed – there will be no level conversion
JP11	3 pins jumper	Define power 3.3V or 5V for the UUT VIO pins. If 1-2 pins are closed then VIO = 5 volts, 2-3 pins are closed then VIO = 3.3 volts
JP1,JP2,JP3,JP8,JP9	Block of Jumpers (5x3)	Define power source for the UUT bus. If 1-2 pins on the all jumpers are closed, then adapter logic and UUT will be powered from Primary PCI. If 2-3 pins on all jumpers are closed, then adapter and UUT will be powered from External Power supply

Table 5: Jumpers

6.5 Connectors

RefDes	Type	Usage
J5	5x2 (2.5 mm) header	Byte blaster connector
J4	DB-25 (male)	Parallel port connector for communication with main computer
J10,J20		PMC bus PN1 and PN2 connectors
J11	6x2 (2.5 mm) header	PCI signals for Logic Analyzer

J12	30x2 (2.5 mm) header	PCI signals for Logic Analyzer
J1	Disk drive power connector	External Power supply connector

Table 6: Connectors

6.6 PMC Connector pin assignment

Pn1 / J10 32-bit PCI				**Pn2 / J20 32-bit PCI**			
Pin	Signal	Signal	Pin	Pin	Signal	Signal	Pin
1	TCK	-12V	2	1	+12V	TRST#	2
3	GND	INTA#	4	3	TMS	TDO	4
5	INTB#	INTC#	6	5	TDI	GND	6
7	BUSMODE1#	+5V	8	7	GND	PCI-RSVD	8
9	INTD#	PCI-RSVD	10	9	PCI-RSVD	PCI-RSVD	10
11	GND	3.3 Vaux	12	11	BUSMODE2#	+3.3V	12
13	CLK	GND	14	13	RST#	BUSMODE3#	14
15	GND	GNT#	16	15	+3.3V	BUSMODE4#	16
17	REQ#	+5V	18	17	PME#	GND	18
19	V(I/O)	AD[31]	20	19	AD[30]	AD[29]	20
21	AD[28]	AD[27]	22	21	GND	AD[26]	22
23	AD[25]	GND	24	23	AD[24]	+3.3V	24
25	GND	C/BE[3]#	26	25	IDSEL	AD[23]	26
27	AD[22]	AD[21]	28	27	+3.3V	AD[20]	28
29	AD[19]	+5V	30	29	AD[18]	GND	30
31	V(I/O)	AD[17]	32	31	AD[16]	C/BE[2]#	32
33	FRAME#	GND	34	33	GND	PMC-RSVD	34
35	GND	IRDY#	36	35	TRDY#	+3.3V	36
37	DEVSEL#	+5V	38	37	GND	STOP#	38
39	GND	LOCK#	40	39	PERR#	GND	40
41	PCI-RSVD	PCI-RSVD	42	41	+3.3V	SERR#	42
43	PAR	GND	44	43	C/BE[1]#	GND	44
45	V(I/O)	AD[15]	46	45	AD[14]	AD[13]	46

47	AD[12]	AD[11]	48	47	M66EN	AD[10]	48
49	AD[09]	+5V	50	49	AD[08]	+3.3V	50
51	GND	C/BE[0]#	52	51	AD[07]	PMC-RSVD	52
53	AD[06]	AD[05]	54	53	+3.3V	PMC-RSVD	54
55	AD[04]	GND	56	55	PMC-RSVD	GND	56
57	V(I/O)	AD[03]	58	57	PMC-RSVD	PMC-RSVD	58
59	AD[02]	AD[01]	60	59	GND	PMC-RSVD	60
61	AD[00]	+5V	62	61	ACK64#	+3.3V	62
63	GND	REQ64#	64	63	GND	PMC-RSVD	64

Table 7: PMC connector pin assignment

7 Appendix A: JTAG Programming Interface

Function	eX10 (2x5) connector (J5)	XILINX FPGA HEADER
VCC (5v- 1.2V)	4	1
TDO	3	4 (D / P)
TDI	9	5 (DIN)
TMS	5	6(PROG)
TCK	1	3(CCLK)
GND	2,10	2

Table 8: JTAG Programming Interface for XILINX

Function	eX10 (2x5) connector (J5)	2x5 Altera connector
VCC (5v- 1.2V)	4	4
TDO	3	3
TDI	9	9
TMS	5	5
TCK	1	1
GND	2,10	2,10

Table 9: JTAG Programming Interface for ALTERA

Function	eX10 (2x5) connector (J5)	1x8 Lattice Download Cable header	1x10 Lattice SPI Flash Programming header
VCC (5v- 1.2V)	4	1	1

TDO	3	2	2(SFLASH_Q)
TDI	9	3	3(SFLASH_D)
TMS	5	6	nc
TCK	1	8	8(SFLASH_C)
ISPEN/BSCAN	8	nc	4(SFLASH_S_N)
RESET	6	nc	nc
GND	2,10	7	7

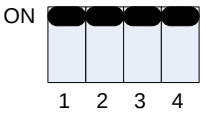
Table 10: JTAG Programming Interface for LATTICE

Function	**eX10 (2x5) connector (J5)**	**TBD**
VCC (5v- 1.2V)	4	TBD
TDO	3	TBD
TDI	9	TBD
TMS	5	TBD
TCK	1	TBD
INI	6	TBD
AF	8	TBD
GND	2,10	TBD

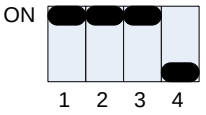
Table 11: JTAG Programming Interface for ATMEL

8 Appendix B: Operation Modes

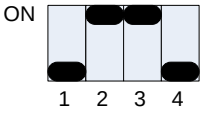
The following table show different operation modes depending of DIP Switch setting:



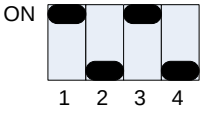
Update logic mode.



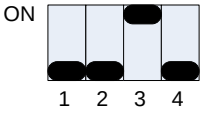
Xilinx JTAG interface mode.



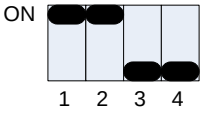
Altera JTAG interface mode.



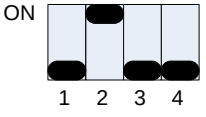
Lattice JTAG interface mode.



ATMEL JTAG interface mode.



SPI interface mode.



I2C JTAG interface mode.

9 Appendix C: High Density Logic Analyzer Connection

The following tables show an example of connection between adapter and high density logic analyzer pods:

J6					J8		
POD 2			POD 1		POD 2			POD 1
+5V	NC	NC	SCL		+5V	NC	NC	SCL
GDC	GND	NC	SDA		GDC	GND	NC	SDA
CLK	NC	NC	CLK		CLK	PCLK	NC	CLK
D15	PCIAD15	PCIAD31	D15		D15	PCLK	DBG1	D15
D14	PCIAD14	PCIAD30	D14		D14	PRST	DBG2	D14
D13	PCIAD13	PCIAD29	D13		D13	REQ	DBG3	D13
D12	PCIAD12	PCIAD28	D12		D12	GNT	DBG4	D12
D11	PCIAD11	PCIAD27	D11		D11	IDSEL	DBG5	D11
D10	PCIAD10	PCIAD26	D10		D10	FRAME	DBG6	D10
D9	PCIAD9	PCIAD25	D9		D9	TRDY	DBG7	D9
D8	PCIAD8	PCIAD24	D8		D8	IRDY	DBG8	D8
D7	PCIAD7	PCIAD23	D7		D7	DEVSEL	LRST	D7
D6	PCIAD6	PCIAD22	D6		D6	STOP	INTD	D6
D5	PCIAD5	PCIAD21	D5		D5	LOCK	INTC	D5
D4	PCIAD4	PCIAD20	D4		D4	INTA	INTB	D4
D3	PCIAD3	PCIAD19	D3		D3	CBE3	PERR	D3
D2	PCIAD2	PCIAD18	D2		D2	CBE2	SERR	D2
D1	PCIAD1	PCIAD17	D1		D1	CBE1	M66EN	D1
D0	PCIAD0	PCIAD16	D0		D0	CBE0	PAR	D0

Table 12: Connection between adapter and high density logic analyzer pods

10 Appendix D: Limited warranty

AMFELTEC Corporation does not warrant that the operation of the hardware, software or firmware products will be uninterrupted or error free. AMFELTEC products are not intended to be used as critical components in life support systems, aircraft, military systems or other systems whose failure to perform can reasonably be expected to cause significant injury to humans. AMFELTEC expressly disclaims liability for loss of profits and other consequential damages caused by the failure of any product which would cause interruption of work or loss of profits, such as shipboard or military attachment.

THIS LIMITED WARRANTY IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED. THE WARRANTIES PROVIDED HEREIN ARE BUYER'S SOLE REMEDIES. IN NO EVENT SHALL AMFELTEC CORPORATION BE LIABLE FOR DIRECT, SPECIAL, INDIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES SUFFERED OR INCURRED AS A RESULT OF THE USE OF, OR INABILITY TO USE THESE PRODUCTS. THIS LIMITATION OF LIABILITY REMAINS IN FORCE EVEN IF AMFELTEC CORPORATION IS INFORMED OF THE POSSIBILITY OF SUCH DAMAGES.

Some states do not allow the exclusion or limitation on incidental or consequential damages, so the above limitation and exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.