32–Bit PCI Bus Extender

Hardware Manual

July 20, 2008

Revision 1.2

Amfeltec Corp.
35 Fifefield dr.
Maple, ON L6A 1J2

www.amfeltec.com

Contents

Figures

Tables

1 About this Document

1.1 Purpose

This document describes Hardware installation, features, specification and operation of AMFELTEC Corp. 32-bit PCI Bus Extender.

1.2 Feedback

AMFELTEC makes every effort to ensure that the information contained in this document is accurate and complete at time of release. Please contact AMFELTEC if you find any errors, inconsistence or have trouble understanding any part of this document.

To provide your feedback, please send an email to support @amfeltec.com

Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	06-01-2005
1.1	Minor changes for hardware design	06-20-2005
1.2	Software manual part moved into separated document.	07-20-2008

2 General Description

2.1 Introduction

The “eX10” PCI bus extender is a Universal high-speed 32 bit PCI bus extender with integrated logic to support debugging and verification of PCI cards (referred as UUT, Units-Under-Test). The UUT is plugged-in to the motherboard slot through the extender.

The extender has a bus switches for support two types of signal environments: 5V and 3.3V. Bus switches also allow you to disconnect the UUT PCI card from the motherboard without shutting down the system (Hot swapping mode). This flexibility minimizes the testing time and protects the motherboard from unexpected damages.

The extender supports two ways of feeding the secondary PCI bus with power: internally, through the motherboard PCI slot, and from an external power supply. The external power supply has to provide 5V and +12V voltages to satisfy all PCI needs:

5V, +12V, -12V, 3.3V and VIO (configurable as 5V or 3.3V).

The extender fully protects your UUT and host system from unpredicted damages by providing both monitoring and limiting of currents and voltages.

The extender includes logic (based on the Xilinx CPLD XC9536XL-10) for debugging and verification purposes:

- FPGA ByteBlaster functionality for the different types of the FPGA (like Xilinx, Altera, Atmel, Lattice) through the external cable
- Master I2C and SPI operations

The CPLD logic can be customized for the client needs. The standard package of the extender includes full schematics and logics for CPLD.

All these functions communicate with the computer through parallel interface. The same interface can be used to update or to load customer’s specific functions into the on- board CPLD.

The extender has two test-point headers of all PCI bus signals for logic analyzer hookup. It has an option of supporting plug-in high density logic analyzer adapters (like Agilent E5339A, E5346A and E5351A). The high-density adapter is specially designed for connection between the Logic Analyzer cables and extender in system where space between PCI cards is limited (required minimal space is 20.32 mm).

The extender supports two types of the computer boxes: standard and 2U profiles. The uniqueness of this mechanical design though that in the both profiles it gives you a perfected access to the bracket-based connectors of your UUT card.

The extender was design based on the many years of development experience and has many features those are very useful for the development and production support of different types of FPGA-based PCI cards.

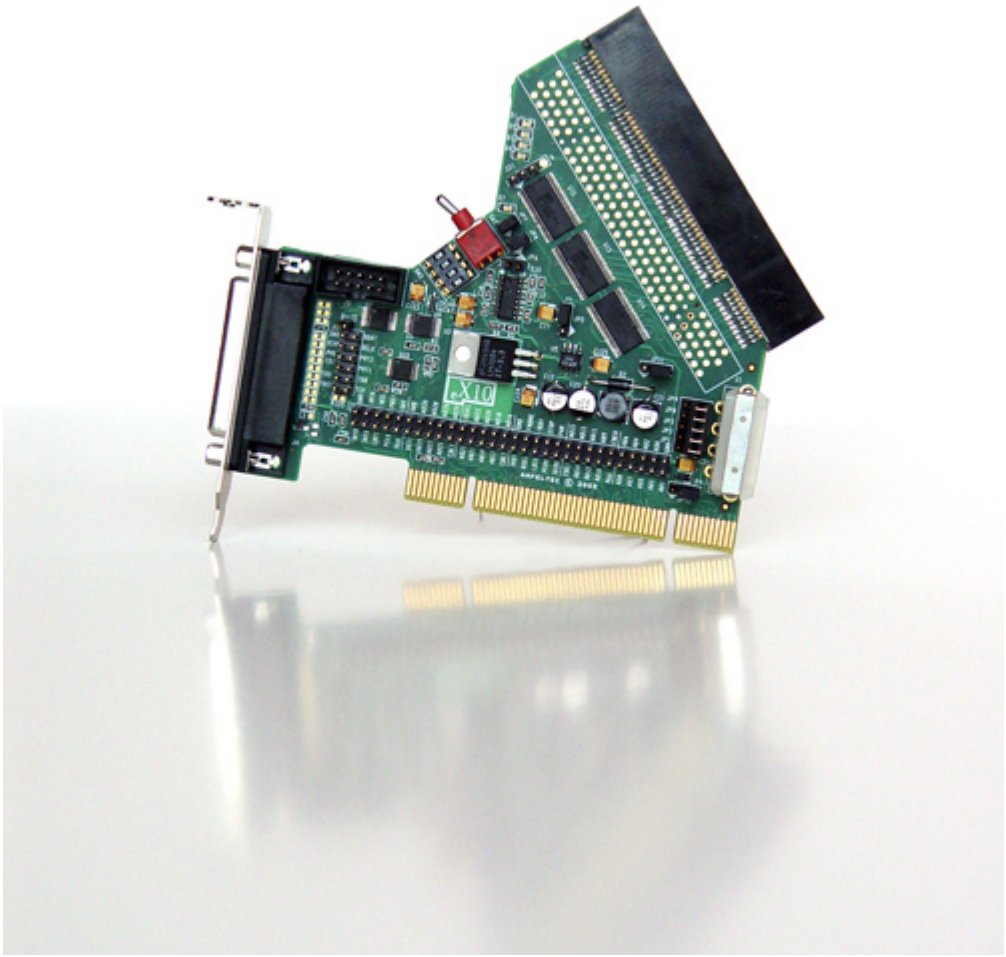


Figure 1: 32-bit PCI Extender

3 Features

3.1 Power

- Visualization of UUT powers - 5 Volt, 3.3V, +12V and – 12V (Green LEDs)
- Overloading Protection (OLP) on the UUT 5V, 3.3V, +12V and -12V supplies
- Under-voltage protection (UVP) on the UUT 5V, 3.3V, +12V
- UUT power failure protection (in case OLP or UVP and indication filer on the LED (red)
- Setting value for UUT VIO power 5V or 3.3V via jumper
- 32 Bit Universal Primary PCI Slot and 5V UUT PCI connector (optionally 3.3V PCI connector)
- eX10 can be powered from primary PCI or from external power supply (define by Jumpers block, can be used any computer power supply with standard IDE interface power connector)
- eX10 implements PCI signal level conversion for connection support of 3.3 V UUT to the 5 V primary PCI bus
- UUT hot swapping capability

3.2 Logic

- Supports ByteBlaster functionality for different FPGAs: Xilinx, Altera, Lattice and Atmel
- Converts parallel interface signals to/from I2C or SPI bus signals
- Supports operation while power up with any voltages from 1.2V – 5.5 V

3.3 Debugging support

- eX10 has 2 brackets to support normal and 2U computer boxes
- All primary PCI signals are connected to 2x2.5 mm header to simplify the testing with Logic Analyzer or Oscilloscope
- An additional adapter supports connection between 2x2.5 mm header and high density HP Logic Analyzer probe
- Make possible the access to the PCI base JTAG interface of the UUT

3.4 Software

- Hot swapping software for saving and restoring PCI configuration for UUT for hot-swap operation (refer to *eX10 Software Manual for more details*)
- I2C master write/read software
- Supported operating systems: Windows, Linux, FreeBSD

3.5 Power limits

Power	Threshold for under voltage monitoring	Maximum current for Over voltage protection	Comments
+3.3V	+2.74V min.	4.8 A	
+5V	+4.42V min.	4.5 A	
+12V	+10.5V min.	0.8 A	
-12V	Not available	0.2 A	In case that extender taking power from PCI connector and PCI connector doesn't provide -12Volt power, jumper JP6 has to be short.

Table 1: Power limits

4 Hardware Description

4.1 Board Layout

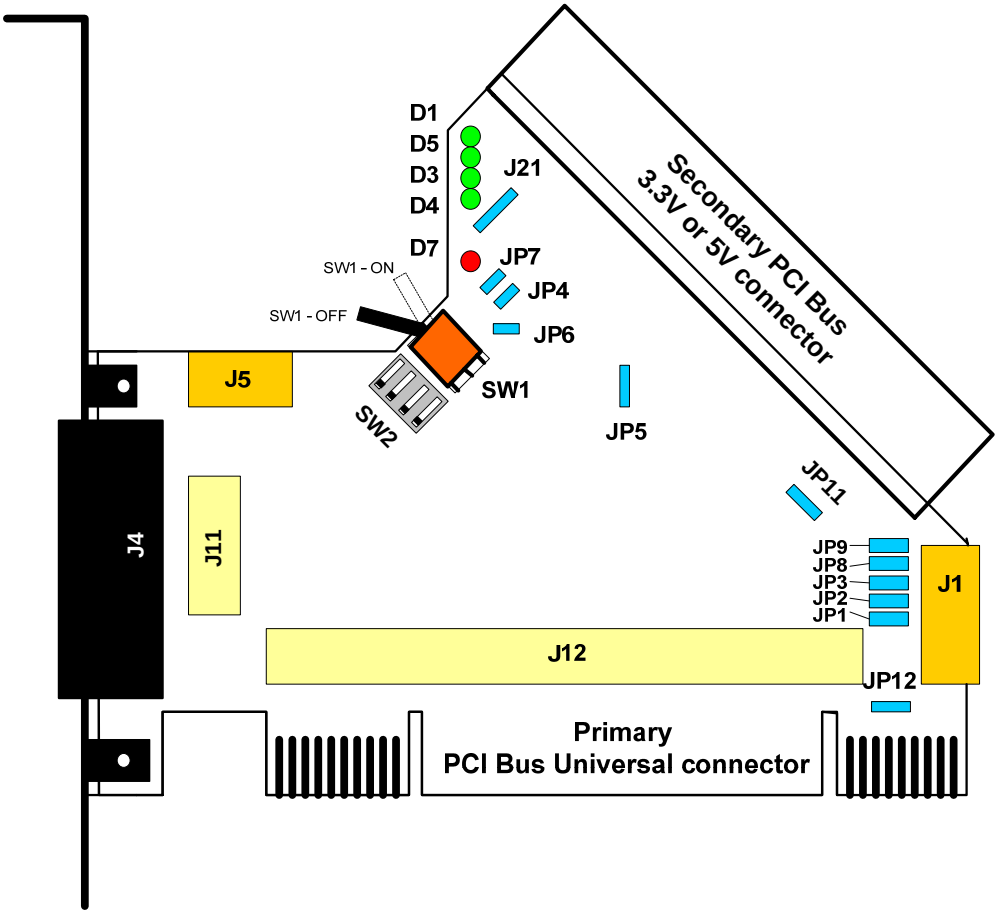


Figure 2: Board Layout

4.2 LEDs

Name	RefDes	Color	Usage
+3.3 Volt	D1	Green	3.3Volt power on the UUT
-12 Volt	D5	Green	-12Volt power on the UUT
+ 5 Volt	D3	Green	+5Volt power on the UUT

+ 12 Volt	D4	Green	+12Volt power on the UUT
+ 5 Volt	D13	Green	+5Volt power for the UUT from Primary PCI or from external connector
Power Fail	D7	Red	UUT power Fail (In case overload or under voltage)

Table 2: LEDs

In case that "Power Fail" LED is ON (overload or under voltage condition happens) it is necessarily to toggle on UUT power switch SW1 for reset fail condition.

4.3 Switch

Name	RefDes	Type	Usage
UUT Power ON/OFF	SW1	Toggle x 1	Power switch for the UUT. In case Power OFF – all PCI signals from the Primary PCI bus are disconnect from the UUT (Hot swapping)
MODE	SW2	Toggle x 4	Four toggle switches define extender logic between Parallel interface and UUT download interface

Table 3: Switch

Follow table shows setting for the different SW2 switch settings.

1	2	3	4	*Usage*
ON	ON	ON	ON	Test mode for update CPLD logic itself (XC9572XL-10VQ44)
ON	ON	ON	OFF	JTAG / Parallel download interface for Xilinx
OFF	ON	ON	OFF	JTAG / Parallel download interface for Altera
ON	OFF	ON	OFF	JTAG / Parallel download interface for Lattice
OFF	OFF	ON	OFF	Download interface for ATMEL
ON	ON	OFF	OFF	Master SPI interface
OFF	ON	OFF	OFF	Master I2C interface
ON	OFF	OFF	OFF	SPARE mode
OFF	OFF	OFF	OFF	SPARE mode

Table 4: Switch SW2

4.4 Jumpers

RefDes	Type	Usage
J21	4 pins jumper	Ground pins for the Test Equipment connection
JP7	2 pins jumper	Has to be close in case to provide -12 Volt power to UUT
JP4	2 pins jumper	Has to be close in case to provide +12 Volt power to UUT

JP6	2 pins jumper	Has to be close in case that UUT power source (Primary PCI or External power supply) doesn't have -12 Volts
JP5	3 pins jumper	1-2 pins have to be connected in case UUT power source (Primary PCI or External power supply) doesn't have +12 Volts
JP12	3 pins jumper	If 2-3 pins are close then all 5 volt signals from Primary PCI will be converting to the 3.3 volts signals. (For support 3.3 volts UUT). In case that 1-2 pins are close – will be no level conversion
JP11	3 pins jumper	Define power 3.3V or 5V for the UUT VIO pins. 1-2 pins are close then VIO = 5 volts, 2-3 pins are close then VIO = 3.3 volts
JP1,JP2, JP3,JP8, JP9	Block of Jumpers (5x3)	Define power source for the UUT bus. If 1-2 pins on the all jumpers are close, then extender logic and UUT will be powered from Primary PCI. If 2-3 pins on all jumpers are closed, then extender and UUT will be powered from External Power supply

Table 5: Jumpers

4.5 Connectors

RefDes	Type	Usage
J5	5x2 (2.5 mm) header	ByteBlaster connector
J4	DB-25 (male)	Parallel port connector for communication with main computer
J11	6x2 (2.5 mm) header	PCI signals for Logic Analyzer
J12	30x2 (2.5 mm) header	PCI signals for Logic Analyzer
J1	Disk drive power connector	External Power supply connector
J10	TH 32 bit PCI connector (optional)	Additional PCI connector for support Right Angel application

Table 6: Connectors

5 Installation

5.1 Hardware Installation

1. To install the PCI extender power off the host computer. The shipped package includes two types of brackets: low and high profile. If you like to change the brackets, you need to unscrew the installed bracket from the connector J4 and replace by another bracket.
2. The ex10 PCI extender is a universal solution for debugging different types of PCI devices. In order to properly configure the extender, please refer to Table 4 (jumpers JP5, JP11, JP12).
3. The extender has integrated Universal ByteBlaster. If you are going to use ByteBlaster, please refer to Table 3 or Appendix B (switch SW2) to set the correct mode of operation.
4. Select power source for UUT. The extender provides two options for selecting proper power source: internal power from the primary PCI bus and external power supply. In order to select the power source, refer to Table 4 (JP1, JP2, JP3, JP8 and JP9).
5. Install the extender into a PCI slot. Important Note: **Secure the extender using a screw in the metal bracket!**
6. Install UUT board into extender.
7. In case you are using external power supply you have to turn it on **first** (before power up the computer). Then, set switch SW1 to position ON (enable power) for secondary PCI bus and UUT.

Now, you can power-up the host computer.

BE SURE THAT FOUR GREEN LEDS (D1, D3, D4 and D5) ARE ON!
In case you see the red led is ON please turn off your computer and check the extender configuration jumpers or UUT device for power shortage.

5.2 Software Installation

For normal operation, you don't need to install additional software. But if you are going to use HOT-SWAP functionality, you need to install eX10 Software Package (refer to *eX10 Software Manual for more details*).

6 Hot-Swap Support

Perform hot swapping with a certain degree of carefulness. Remember that PCI configuration won't be loaded or automatically updated on insertion of a new UUT device unless you use the supplied *eX10 Software Package* that provides HOT-SWAP feature to reload the UUT's PCI configuration.

IMPROPER USE OF HOT-SWAP FEATURE CAN CAUSE THE SYSTEM TO CRASH OR THE SYSTEM CAN BECOME UNSTABLE!

6.1 Remove UUT Device

The following steps describe detail sequence for removing UUT device:

1. On fully operated systems save UUT PCI configuration into a file
2. Unload all device drivers from the system that are using your UUT device
3. Set the switch SW1 to "OFF" (disable power)
4. Now, you can remove UUT device from the secondary PCI connector

6.2 Install UUT Device

The following steps describe detail sequence for installing UUT device back to the system:

1. Verify that SW1 is in position "OFF"
2. Plug in UUT device into the secondary PCI connector
3. Set the switch SW1 to "ON" (enable power)
4. Restore PCI configuration for the UUT device

Now, the UUT device is ready for use!

7 Appendix A: JTAG Programming Interface

Function	eX10 (2x5) connector (J5)	XILINX FPGA HEADER
VCC (5v- 1.2V)	4	1
TDO	3	4 (D / P)
TDI	9	5 (DIN)
TMS	5	6(PROG)
TCK	1	3(CCLK)
GND	2,10	2

Table 7: JTAG Programming Interface for XILINX

Function	eX10 (2x5) connector (J5)	2x5 Altera connector
VCC (5v- 1.2V)	4	4
TDO	3	3
TDI	9	9
TMS	5	5
TCK	1	1
GND	2,10	2,10

Table 8: JTAG Programming Interface for ALTERA

Function	eX10 (2x5) connecto r (J5)	1x8 Lattice Download Cable header	1x10 Lattice SPI Flash Programming header
VCC (5v- 1.2V)	4	1	1
TDO	3	2	2(SFLASH_Q)
TDI	9	3	3(SFLASH_D)
TMS	5	6	nc
TCK	1	8	8(SFLASH_C)
ISPEN/BSCAN	8	nc	4(SFLASH_S_N)
RESET	6	nc	nc
GND	2,10	7	7

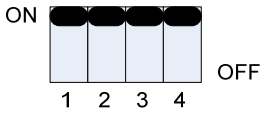
Table 9: JTAG Programming Interface for LATTICE

Function	eX10 (2x5) connector (J5)	TBD
VCC (5v- 1.2V)	4	TBD
TDO	3	TBD
TDI	9	TBD
TMS	5	TBD
TCK	1	TBD
INI	6	TBD
AF	8	TBD
GND	2,10	TBD

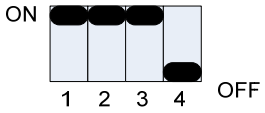
Table 10: JTAG Programming Interface for ATMEL

8 Appendix B: Operation Modes

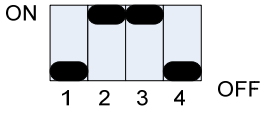
The following table shows different operation modes depending of DIP Switch setting:



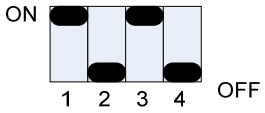
Update logic mode.



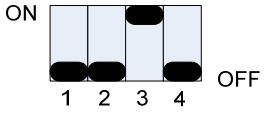
Xilinx JTAG interface mode.



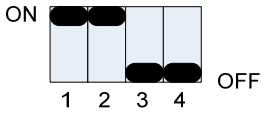
Altera JTAG interface mode.



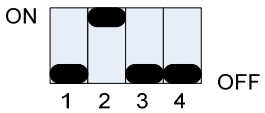
Lattice JTAG interface mode.



ATMEL JTAG interface mode.



SPI interface mode.



I2C JTAG interface mode.