PCI Express Test Backplane

Hardware Manual

January 28, 2013

Revision 1.3

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1 About this Document

1.1 Purpose

This document describes hardware installation, features, specification and operation of the AMFELTEC Corp. PCI Express Test Backplane.

1.2 Feedback

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Your comments or corrections are greatly valued in our effort for excellence and continued improvement.

1.3 Revision History

Rev. No.	Description	Rev. Date
1.0	Initial Release.	September 15, 2008
1.1	Minor modification	November 10, 2010
1.2	Minor modification for appendix B	June 14, 2011
1.3	Minor modification	January 28, 2013

2 General Description

2.1 Introduction

The "PCI Express Test Backplane" (backplane) is a four slot PCI express backplane (3 slots with x1 PCI Express connectors and one x4 PCI Express connector) that connects to the upstream host computer via two cables (standard CAT6 and 10 wires flat cables) and x1 PCI express host board. The host board has to be plugged into the PCI express connector on the motherboard of the upstream host computer. The Backplane supports debugging, verification as well as production testing and programming of PCI express based boards. Using the backplane eliminates the risk of damage to the host computer during debugging, programming and testing PCI boards and at the same time the host computer can be removed from the testing area to free up space.

By using the PCI express hot-swap power controllers (one per PCI express slot) the power of each PCI express slot can be shutdown due to the overcurrent protection and in this case doesn't effect the other PCI express slots on the backplane or upstream host computer. The SW1 local power switch controls all 4 power-controllers and can power down local PCI express slots without any effect to the upstream host computer. This allows easy replacement of plugged in PCI express boards (referred UUT, Unit-under-Test) on the backplane and significantly decreases testing/verification time.

All four PCI Express connectors are powered from separate Hot-swap power controllers. Those power controllers are independent and have over current protection and under voltage protection. Thus all UUTs and host system are fully protected from damage in case of power shortage. Each slot has additional auxiliary power connector (GND, +12 Volts and +3.3 Volts) to provide per slot power to the external devices (UUTs) connected to the test backplane.

 The "PCI Express Test Backplane" has four JTAG connectors (one for each PCI express slot) to provide access from an external programmer/emulator to the PCI bus JTAG signals. This feature is unique and not found on other PCI backplanes or motherboards. It gives the possibility to run JTAG production tests, use a JTAG emulator for UUT debugging and/or to use **"eLoader"™** from AMFETLEC Corp. for programming/loading CPLD/FPGA on the UUT during debugging or production cycle.

The backplane has surface-mount LEDs which provide a convenient visual check for the main powers (+12V, +3.3V, +5VSB), status of the power controllers per PCI Express slot (Power ON/OFF, power GOOD/FAIL) and status of the upstream PCI express connection.

An additional "PCI Express Test Backplane" has two support tabs for mechanical stabilization of add-in PCI express boards (U.S. Patent 7,255,750).

2.2 Package Details

The PCI Test Backplane includes following components:

1. PCI Test Backplane (Figure 1)

2. PCI express host board (Figure 2)

3. Data CAT6 cable and control flat cable (both cables 7 ft.)

4. User manual

Figure 1: PCI Express Test Backplane

Figure 2: PCI express host board

3   Requirements/Features

3.1   Power/Interface signals

- Visualization of UUT power status +3.3V, +12V, +5VSB (Green LED)

- Overloading Protection (OLP) on the UUT +3.3V and +12V supplies

- Under-voltage protection (UVP) on the UUT +3.3V and +12V

- UUT power failure protection (in case OLP or UVP), failure is indicated by red LED per PCI Express slot

- Backplane is powered from external standard ATX power supply. (standard ATX 20/24 pin power connector)

- Meets PCI Express Bus Specification 1.1.

- Supports hot-swapping of all four UUTs without shutting down host computer

3.2   Debugging support

- Allows access to the PCI Express JTAG interface of each of the four UUTs

3.3   Mechanical stabilization for PCI Express Boards

PCI Express Test Backplane has two support tabs for mechanical stabilization of add-in PCI express boards (Figure 3).
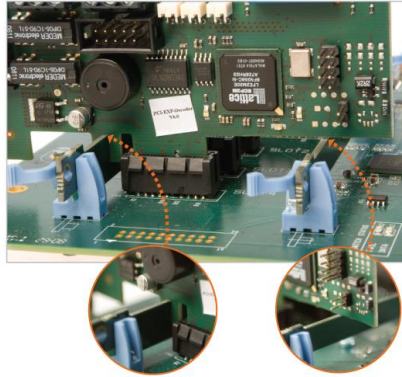
Figure 3: Mechanical stabilization for PCI Express Boards

3.4 Software

AMFELTEC Corp. provides software for supporting how-swap functionality. The software allows to save and restore the PCI Express configuration for UUT device (refer to *eX10 Software Manual for more details*).

4 Installation

4.1 Hardware

Following steps provide the exact sequence that needs to be followed in order to properly install the PCI Express Test Backplane product from AMFELTEC Corp.:

- Turn OFF host computer before installation.

- Remove the chassis cover from host computer.

- Locate an unused PCI express slot and remove the corresponding slot cover from computer chassis.

- Plug-in the x1 PCI express host board to selected PCI express slot and attach its bracket to the computer chassis with a screw.

- Put the chassis cover back on the computer.

- Connect the CAT6 cable and flat cable to PCI express Host Board and the other end to the connectors on the PCI Express Test Backplane.

- Connect the ATX power supply to the PCI Express Test Backplane.

- Check JP21and SW1 setting on the PCI Express Test Backplane.

- Turn power switch ON for the ATX power supply. LED D5 (STBY) indicates that the stand by power is present and that it's ready for operation.

- If jumper JP21 is set in position 2-3 (backplane power will be switch ON/OFF by powering host computer) then you can turn on the host computer (Please check position of the SW1. It has to be in position ON if you need to supply power for the local 4 PCI express slots on the backplane).

- If jumper JP21 is set in position 1-2 (backplane power will be controlled by push button S2). Turn backplane power ON by toggling push button S2. Please check position of SW1. It has to be in the ON position if you need to supply power to the local 4 PCI express slots on the backplane. Then you can turn on the host computer.

- When the system is booted, you can install the software.

<u>NOTE</u>:

1. We recommend adding additional ground connection to the Host PC and to the ATX power supply.

2. Some of the ATX power supplies require a minimum load on the 12Volt line to achieve stability. If the installed UUTs don't draw much power from 12V line, this minimum load might not be met. The additional load module is available from Amfeltec Corp.

4.2   Software

PCI Express Test Backplane doesn't require any software/device driver for operation. You will only need to install the software provided by AMFELTLEC Corp. in order to use the hot-swap feature.

Please refer to eX10Suite Manual for software installation details.

5 Operation

5.1 Hot-Swap Support

Perform hot swapping with a certain degree of carefulness. Remember that PCI configuration won't be restored automatically after insertion of a new UUT device unless you use the supplied HOT SWAP software to reload the UUT's PCI configuration.

5.1.1 Remove UUT Device

The following steps describe the sequence for removing UUT device:

1. Save UUT PCI configuration into a file (refer to Software Manual for *more details)*.

2. Unload all device drivers associated with the UUT.

3. Set the switch SW1 to "OFF" (disable power).

Now, you can remove UUT device from any of the 4 local PCI express slots on the backplane.

5.1.2 Install UUT Device

The following steps describe the sequence for installing UUT device back to the system:

1. Plug in UUT device into original PCI express slot on the backplane (If you are using multiple UUT devices, please install these device into original PCI express slot positions).

2. Set the switch SW1 to "ON" (enable power).

3. Restore PCI configuration for the UUT device.

Now, the UUT device is ready for use.

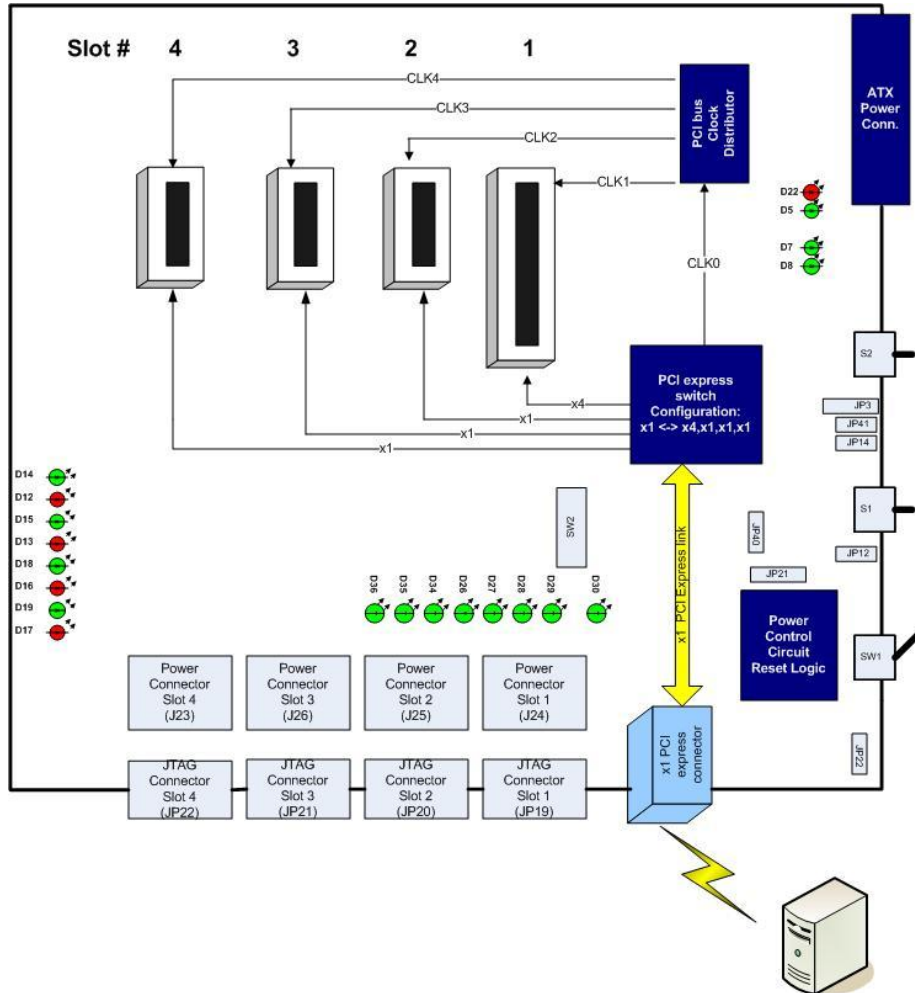# 6   Hardware Description

6.1   Board Layout

Figure 4: Board layout

6.2   LEDs

Name	Ref. Des.	Color	Usage
LRST	D22	RED	Local RESET signal indicator
STBY	D5	GREEN	Power Supply stand by power indication
3.3V	D7	GREEN	+ 3.3V local power on the backplane
+12V	D8	GREEN	+ 12V local power on the backplane
Ext. LINK	D30	GREEN	Upstream PCI express link status indicator
Slot 1/Link 3	D29	GREEN	PCI express link status for the first PCI Express slot
Slot 1/Link 2	D28	GREEN	PCI express link status for the first PCI Express slot
Slot 1/Link 1	D27	GREEN	PCI express link status for the first PCI Express slot
Slot 1/Link 0	D26	GREEN	PCI express link status for the first PCI Express slot
Slot 2/Link 5	D36	GREEN	PCI express link status for the PCI Express slot 2
Slot 3/Link 6	D35	GREEN	PCI express link status for the PCI Express slot 3
Slot 4/Link 7	D34	GREEN	PCI express link status for the PCI Express slot 4
Ext. LINK	D30	GREEN	Upstream PCI express link status indicator
PWR	D14	GREEN	Power status on the slot number 1
FAIL	D12	RED	Power Fail on the slot number 1 (In case overload or under voltage)
PWR	D15	GREEN	Power status on the slot number 2
FAIL	D13	RED	Power Fail on the slot number 2 (In case overload or under voltage)
PWR	D18	GREEN	Power status on the slot number 3
FAIL	D16	RED	Power Fail on the slot number 3 (In case overload or under voltage)
PWR	D19	GREEN	Power status on the slot number 4
FAIL	D17	RED	Power Fail on the slot number 4 (In case overload or under voltage)

Table 1: LEDs

6.3 Switches

Follow table shows settings for the PCI Express Test Backplane switches:

Name	Ref. Des.	Type	Usage
BACKPLANE POWER	SW1	Switch	Power switch for all 4 PCI Express slots. In case OFF state – the power on all 4 PCI Express slots is off. UUT boards can be replaced. (Hot swap mode)
PWR ON	S2	Push Button	"PWR ON" push button switch ON ATX power supply in case that JP21 in position 1-2. (Local backplane Power supply control)
RESET	S1	Push Button	"RESET" push button provides RESET signal for the local PCI Express bus.

Table 2: Switches

6.4 Jumpers

Ref. Des.	Type	Usage
JP40	2 pins jumper	Local mode enable in case run PCI Express Test backplane without upstream connection.
JP21	3 pins jumper	If 1-2 pins closed, then backplane ATX power supply is controlled by S2 (local control). If 2-3 pins are closed, then backplane ATX power supply is controlled by host computer. (Power On host computer automatically switch power on the backplane).

Table 3: Jumpers

6.5 Connectors

Ref. Des.	Type	Usage
JP3	3 pins connector	External Power LED connection. (In parallel with D6)
JP41	2 pins connector	External RESET LED connection. (In parallel with D22)
JP14	2 pins connector	External RESET push button. (In parallel with S1)
JP12	2 pins connector	External Power ON / OFF push button connection. (In parallel with S2)
J19,J20, J21,J22	5x2 (2.5 mm) header	JTAG emulator/programmer connection. Direct connection to the "eLoader ™" from Amfeltec Corp. (per PCI slot)
J11,J12, J13,J14	Standard PCI Express connectors	Three x1 PCI express connectors and one x4 PCI express connector.
J7	Standard ATX power supply 24 pin connector	Connector for ATX power supply. (Supplies power for PCI Express Test Backplane).
J10	5x2 (2.5 mm) header	Connector for control cable between PCI Express Test Backplane and host computer.
J9	RJ45 connector for the PCI express cable connection	Connector for CAT6 cable between PCI Express Test Backplane and host computer.

Table 4: Connectors

6.6   Power Limits per Slot

Power	Maximum current
+3.3V	4.9 A
+12V	0.8 A

Table 5: Power Limits

7   Appendix A: JTAG Programming Interface

Function	JTAG connector
TCK	1
N/C	2
TDO	3
VIO (power out)	4
TMS	5
N/C	6
TRST	7
N/C	8
TDI	9
GND	10

Table 6: JTAG connectors J19, J20, J21 and J22

8   Appendix B: DIP Switch

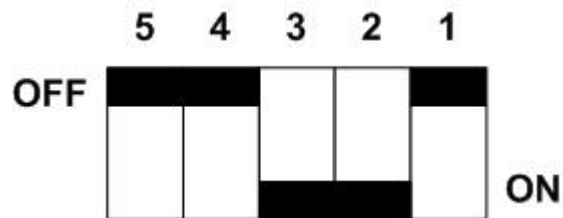Picture of the DIP Switch setting in the normal operation mode:

Table 7: DIP switch

9   Appendix C: Limited warranty

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